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# MEMORY ARRAY

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## CROSS-REFERENCE TO RELATED APPLICATION

This application is related to co-pending and commonly assigned applications
serial number _____, filed _____ (attorney docket  no. 200309680)
and serial number _____, filed _____ (attorney docket

15    no. 200311564), the entire disclosure of each of which is incorporated herein
by reference.

## TECHNICAL FIELD

This invention relates generally to arrays of memory devices and methods for
their fabrication.

20    ## BACKGROUND

Markets for computers, video games, televisions, portable telephones, PDAs
and other electrical devices are requiring increasingly larger amounts of memory
to store images, photographs, videos, movies, music, and other storage-
intensive data.  At the same time, as computer and other electrical equipment

25    prices continue to drop, the manufacturers of storage devices, such as memory
devices and hard drives, need to lower the cost of their components.  Thus, in
addition to the need to increase the storage density of their devices,

manufacturers of storage devices must also reduce costs. This trend of
increasing memory storage density while reducing the fabrication costs of the
storage has been on-going for many years. There is accordingly a need for
economical, high capacity memory structures and economical methods for

5    fabricating such structures, especially methods that are compatible with
methods used to fabricate other elements of integrated circuits.

Integrated circuits including arrays of memory nodes or logic gates have also
increased steadily in density. Such integrated circuits have included dynamic
random access memory (DRAM) devices, static random access memory

10   (SRAM) devices, programmable read-only memory (PROM) integrated circuits,
electrically erasable programmable read-only memory (EEPROM) integrated
circuits, write-once read-many (WORM) memory devices, and logic devices
such as programmable logic array (PLA) integrated circuits, among others.

For controlling write and read operations of multi-layer memory arrays, a control

15   element is generally associated with each memory cell of the array. In many
cases, such control elements have required excessive power and have limited
array performance. In some cases, the driver circuits for such control elements
have required relatively large areas, accounting for about half of the array size.

Tunnel-junction control elements using selected area ratios have required

20   smaller areas, but have required additional mask steps for their fabrication, and
have suffered yield losses due to mismatches of tunnel junctions, thus
increasing costs.

When the sense lines within a memory array are each connected to a selected
memory cell and to many other unselected memory cells, and the unselected

25   memory cells are also connected to unselected bit lines, the many parallel paths
through the unselected memory cells from a sense line to the unselected bit
lines are generally referred to as "sneak paths." Thus, currents that flow
through the sneak paths (i.e., "sneak-path currents") have occurred in some
arrays, adversely affecting the performance of read operations.

30   Three-terminal memory cell devices, having a gate electrode for controlling the
state of the memory cell, are known. Many of these are "flash" devices, which

utilize current injection into floating gates. In a typical flash memory, each of the memory cells includes a floating-gate field-effect transistor capable of holding a charge, and the data stored in a cell is determined by the presence or absence of the charge in the floating gate. Other three-terminal memory cell devices

5    employ Metal-Oxide-Nitride-Oxide-Silicon (MONOS) structures or Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) structures in which a gate insulating layer between a channel region and a control gate includes a laminated portion consisting of a silicon oxide layer, a silicon nitride layer, and another silicon oxide layer, and in which the silicon nitride layer traps electric charges. While

10   these memory devices perform their intended functions, there is an on-going need for economical high-yield methods for fabricating memory structures, including memory arrays, especially memory arrays with reduced susceptibility to sneak-path currents.


15   BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the disclosure will readily be appreciated by persons skilled in the art from the following detailed description when read in conjunction with the drawings, wherein:

FIG. 1 is a top plan view of an embodiment of a crosspoint memory array.

20   FIG. 2 is a cross-sectional side elevation view of a first embodiment of a memory cell.

FIG. 3 is a cross-sectional side elevation view of a second embodiment of a memory cell.

FIG. 4 is a cross-sectional side elevation view of a third embodiment of a

25   memory cell.

FIG. 5 is a cross-sectional side elevation view of a fourth embodiment of a memory cell.

FIG. 6 is a cross-sectional side elevation view of a fifth embodiment of a memory cell.

FIG. 7 is a cross-sectional side elevation view of a sixth embodiment of a memory cell.

FIG. 8 is a cross-sectional side elevation view of a seventh embodiment of a memory cell.

5 FIG. 9 is a graph of current/voltage relationships in an embodiment of a memory cell.

FIG. 10 is a graph of resistance vs. current in an embodiment of a memory cell.

FIG. 11 is a cross-sectional side elevation overall view of an embodiment of a memory array.

10 FIG. 12 is a top plan view illustrating an embodiment of a chip layout for a memory array.

FIG. 13 is a schematic block diagram of an embodiment of a row configuration for a memory array.

FIG. 14 is a simplified schematic diagram of an embodiment of a memory array, 15 illustrating a write operation.

FIG. 15 is a simplified schematic diagram of an embodiment of a memory array, illustrating a read operation.

FIG. 16 is a flow chart illustrating an embodiment of a method for fabricating a memory array.

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DETAILED DESCRIPTION OF EMBODIMENTS

For clarity of the description, the drawings are not drawn to a uniform scale. In particular, vertical and horizontal scales may differ from each other and may vary from one drawing to another. In this regard, directional terminology, such 25 as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the drawing figure(s) being described. Because components of the invention can be positioned in a number of different

orientations, the directional terminology is used for purposes of illustration and is in no way limiting.

Integrated circuits having arrays of devices, gates, or memory nodes disposed on multiple levels require "vertical" interconnections or "pillars" to interconnect
5   devices, gates, or memory nodes on one level with other devices, gates, or nodes on other levels. In this context, the term "vertical" differs from its everyday connotation in that it does not refer to the direction of gravity. Throughout this specification, the drawings, and the appended claims, the term "vertical" refers to a direction generally perpendicular to a substrate or base plane of an
10  integrated circuit. Also, the term "pillar" referring to an interconnection and the term "vertical interconnection" are used interchangeably to mean an interconnection communicating between different layers of an integrated circuit, regardless of the spatial orientation of those different layers. Integrated circuits herein include not only monolithic integrated circuits, but also hybrid integrated
15  circuits and multi-layer or "stacked" modules. The term "cell" herein refers to a functional element of an array, such as a memory node, a logic gate, a switching device, a field-effect device, or a semiconductor device.

According to one aspect of the embodiments of the invention, a memory array
20  has a number of row conductors and a number of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and the memory array has a memory cell disposed at each cross-point, as shown in FIG. 1, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each
25  control element including a silicon-rich insulator. The silicon-rich insulator (e.g. silicon-rich oxide) may be patterned. FIG. 1 is a top plan view of an embodiment of such a crosspoint memory array **10**, with a memory cell **20** at each cross-point, row conductors **30**, and column conductors **40** intersecting the row conductors at each memory cell **20**. As shown in FIG. 1, the row
30  conductors **30** may be arranged in mutually orthogonal relationship with the column conductors **40**. Memory cell **20** may be a write-once/read-many device.

Another aspect of the embodiments provides a memory array **10** in which the control element of each cell includes a tunnel junction in addition to the silicon-rich insulator, as shown in FIG. 2. The storage element of each cell may comprise, for example, an anti-fuse, a tunnel junction, or a state-change layer.

5   Specifically, when the storage element comprises a state-change layer, the state-change layer of such a storage element may comprise a chalcogenide.

Various embodiments of memory cell 20 are shown in FIGS. 2 – 8. The cross-sectional views of FIGS. 2, 3, and 4 are all taken at the plane indicated in FIG. 1 for FIG. 2. Dimensions L1 – L8 in the drawings are explained below in the

10  section titled "FABRICATION."

FIG. 2 is a cross-sectional side elevation view of an embodiment of a memory cell **20**. In the embodiment of FIG. 2, column conductor **40** extends to the left and right, parallel to the plane of the drawing. Row conductor **30** extends in a direction perpendicular to the plane of the drawing. The projected intersection

15  of the row and column conductors generally defines the area of memory cell **20** disposed at that intersection. In the embodiment shown in FIG. 2, storage element **50** may be a tunnel junction or a state-change layer such as a chalcogenide layer. In this embodiment, the control element (coupled in series with the storage element) consists of silicon-rich insulator **60** and tunnel junction

20  **70**. Arrow **80** shows the direction of storage-element electron flow. Arrow **90** shows the direction of control-element electron flow. Arrow **100** shows the direction of programming current. As shown in FIG. 2, silicon-rich insulator **60** may be patterned. An optional layer of interlayer dielectric **120** deposited and then planarized to the top of silicon-rich insulator **60** may be used to provide

25  insulation between the individual regions of silicon-rich insulator **60** in various memory cells. Thus, the patterned silicon-rich insulator **60** of each memory cell is electrically isolated from the patterned silicon-rich insulators of all other memory cells. Alternatively, layer **120** can be omitted and layer **70** serves as the insulator between laterally adjacent patterned silicon-rich insulators **60**.

30  It is not necessary to pattern storage layer **50** and control element tunnel-junction layer **70**, since they effectively have infinite resistance between cross-

points.  Silicon-rich insulator layer **60** is a voltage-dependent conductive layer, ideally patterned to avoid the necessity of a constraint on voltage across it between cross-points.  However, it can be optionally un-patterned, if the electric potential across it between cross-points is constrained in the application to be

5    below a specified voltage threshold of conduction.

Thus, another aspect of the embodiments is a memory array **10** including a number of row conductors **30** and a number of column conductors **40** arranged to cross at cross-points, and including a memory cell **20** disposed at each cross-point, each memory cell having a storage element **50** and a control element **45**

10    coupled in series between a row conductor and a column conductor.  Each storage element **50** comprises a tunnel-junction anti-fuse or a state-change layer such as a chalcogenide layer.  Each control element **45** comprises a silicon-rich insulator **60** (optionally patterned) and a tunnel junction **70**.  The silicon-rich insulator **60** of the control element **45** injects current into the tunnel

15    junction **70** of the control element when the memory cell **20** is selected and isolates the storage element **50** when the memory cell **20** is unselected.  Silicon-rich insulator **60** may be considered an electronic switch that allows selection of the memory cell for programming and sensing of the storage state, as well as isolation of the memory cell when the memory cell is unselected.

20    The layer **60** of silicon-rich oxide (SRO) of the control element **45** provides for enhanced current injection into the dielectric of tunnel junction layer **70**. Current injection from SRO is described in the paper by D. J. DiMaria et al., J. Appl. Phys. V. 51(15), May 1980, pp. 2722 – 2735; in the paper by D. J. DiMaria et al., J. Appl. Phys. V. 55(8), 04-15-1984, pp. 3000 – 3019; and in the

25    chapter by D. J. DiMaria, "High Current Injection Into $SiO_2$ Using Si-rich $SiO_2$ Films and Experimental Applications" in "The Physics of MOS Insulators," (G. Lucovsky et al., Eds.) Pergamon Press, New York, 1980, pp. 1 - 18.  The entire disclosure of each of these three publications is incorporated herein by reference.

30    One effect of the silicon-rich-insulator control element of each memory cell is improved isolation and a resultant significant reduction of cumulative sneak-path

currents that might otherwise occur when a row of the memory array is driven. This improved isolation, in turn, allows elimination of very large row-driver circuits, saving up to half of the memory area previously dedicated to row drivers. Each memory cell is electrically isolated from the patterned silicon-rich

5     insulators of all other memory cells. In addition, the size of sub-arrays is substantially increased, which reduces overall overhead for memory array support circuitry. Patterning the memory cell can maximize the achievable array size and can minimize support-circuit overhead costs. This patterning can be achieved with a reduced number of masks or without additional masks, thus

10    lowering fabrication costs. Stacked memory-array layers may be fabricated without destroying lower-layer memory cell structures and lower-layer metal lines. Furthermore, a large part of the area under the array can be utilized for CMOS control circuits, as described below in connection with the discussion of FIG. 11.

15    In comparison with previous solutions, other advantages provided by the use of a silicon-rich insulator include higher currents at the low voltages needed for lower voltage devices and higher current densities which are particularly useful with devices having dimensions below 0.5 micrometer. In addition, the silicon-rich insulator can act like a control element due to its asymmetric rectification

20    characteristic.

Within the control element of the present invention, current injection from the silicon-rich insulator allows the use of thicker oxide, so that fewer defects occur and yield is improved. Also, the breakdown voltage of the control element is improved, significantly reducing the probability of control element failure due to

25    an over-voltage condition that can occur when an anti-fuse changes state.

When storage element **50** is a tunnel-junction oxide or a state-change layer such as a chalcogenide layer, data may written into memory cell **20** by forming a low-resistance filament **110**, shown schematically in FIGS. 2 – 7. While a stylized schematic depiction of low-resistance filament **110** is shown in several

30    embodiments, its shape or its presence in these drawings should not be

regarded as limiting the invention. Otherwise similar embodiments which do not form such a filament are also operable in accordance with the present invention.

FIG. 3 is a cross-sectional side elevation view of a second embodiment of a memory cell. In this embodiment, it is not necessary that silicon-rich insulator

5    layer **60** be patterned, though it may be patterned if desired. A patterned conductive middle electrode **130** effectively determines the portion of silicon-rich insulator layer **60** that participates in operation of the memory cell. The patterned conductive middle electrodes **130** of different adjacent memory cells are insulated from each other by interlayer dielectric (ILD) **120**. In this

10   embodiment, middle electrode **130** is disposed between storage element **50** and silicon-rich insulator layer **60**.

FIG. 4 is a cross-sectional side elevation view of a third embodiment of a memory cell. This embodiment is similar to the embodiment of FIG. 3 in that it has a patterned conductive middle electrode **130**, but this embodiment omits the

15   interlayer dielectric **120**. The silicon-rich insulator **60** insulates different memory cells at adjacent cross-points from each other. In this embodiment, middle electrode **130** is disposed generally between storage element **50** and silicon-rich insulator layer **60** by virtue of being embedded in the bottom portion of the latter. In a variation on the embodiment of FIG. 4, the silicon-rich insulator layer

20   **60** may also be patterned, similarly to the configuration shown in the embodiment of FIG. 2. Also, as in FIG. 2, an interlayer dielectric **120** may be used in conjunction with the patterned silicon-rich insulator layer **60**.

The cross-sectional views of FIGS. 5, 6, 7, and 8 are all taken at the plane indicated in FIG. 1 for FIG. 5. FIG. 5 is a cross-sectional side elevation view of

25   a fourth embodiment of a memory cell. This embodiment is similar in some respects to the embodiment of FIG. 4, but conductive middle electrode **130** is omitted in this embodiment. The directions of storage-element electron flow **80**, control-element electron flow **90**, and programming current **100** in this embodiment are reversed from those of FIGS. 2 - 4. Again, a related

30   embodiment may include a patterned silicon-rich insulator layer **60** and may

also include an interlayer dielectric **120** used in conjunction with the patterned silicon-rich insulator layer **60**, as described in connection with FIG. 2.

FIG. 6 is a cross-sectional side elevation view of a fifth embodiment of a memory cell. In the embodiment shown in FIG. 6, conductive middle

5    electrode **130** is disposed between silicon-rich insulator layer **60** and storage-element layer **50**. The patterned conductive middle electrodes **130** of memory cells at adjacent cross-points are insulated from each other by interlayer dielectric (ILD) **120**. The directions of storage-element electron flow **80**, control-element electron flow **90**, and programming current **100** in this embodiment and

10    that of FIG. 7 are the same as in FIG. 5 (i.e., reversed from those of the embodiments shown in FIGS. 2 – 4).

FIG. 7 is a cross-sectional side elevation view of a sixth embodiment of a memory cell. This embodiment has a patterned conductive middle electrode **130** disposed between silicon-rich insulator layer **60** and storage-element layer

15    **50**, by virtue of being embedded in the bottom portion of the latter. As in all the embodiments of FIGS. 3 – 6, the embodiment of FIG. 7 may be modified in that the silicon-rich insulator layer **60** may also be patterned, similarly to the configuration shown in the embodiment of FIG. 2. Also, as in FIG. 2, an interlayer dielectric **120** may be used in conjunction with the patterned silicon-

20    rich insulator layer **60**.

FIG. 8 is a cross-sectional side elevation view of a seventh embodiment of a memory cell. This embodiment has a conductive middle electrode **130** formed by a final patterning step without a separate mask, thus eliminating a mask step in the fabrication of this embodiment. In the fabrication of this embodiment, a

25    blanket conductive layer **130** is deposited over silicon-rich insulator layer **60**, patterned with the row conductor **30** below it, and storage element layer **50** is deposited over the conductive layer **130**. After column conductor **40** is deposited and patterned, a step of plasma oxidation is performed, using column conductor **40** as a hard mask and oxidizing the unmasked portions of the

30    conductive layer **130** to form oxide regions **140**. Arrows **150** illustrate schematically the oxygen plasma penetration through storage element layer **50**.

The masked portions under column conductor **40** remain un-oxidized and thus remain conductive to form a patterned, isolated, middle electrode **130**.

FIG. 9 is a graph of tunnel-junction current/voltage relationships in an embodiment of a memory cell. The vertical axis shows current, and the
5   horizontal axis shows the tunnel-junction voltage. Read load line **205** and write load line **235** are shown as dashed lines which intersect the voltage axis at read voltage **255** and write voltage **265** respectively, as indicated along the voltage axis. The low-conductivity-state read current is indicated by horizontal dashed line **206**. The high-conductivity-state read current is indicated by
10  horizontal dashed line **207**. As voltage across an un-fused (effectively open) tunnel-junction device is increased (curve **250**), typically, the tunnel junction fuses at a switch point **275**, whereupon a complete filament is formed and the current-voltage characteristic changes (arrow **260**) to that of a fused (effectively shorted) device, shown by line **240**. After a fusing event is completed, the
15  current-voltage characteristic **240** of the fused tunnel-junction device falls within a fairly narrow sensing-voltage range. The two arrows **241** and **242** represent retrace of current along the current-voltage characteristic in the high-conductivity state. It should be noted that the high conductivity state retraces but the low conductance state does not; once the device switches, the current
20  follows only the nearly vertical line **240**. In those devices that are not switched, the current follows the leftmost portion of current-voltage characteristic **250**.

Memory cell embodiments employing a control element with both a silicon-rich insulator and a tunnel junction are improved in uniformity and reliability over those with only a tunnel-junction control element. FIG. 10 is a graph of total
25  resistance (Megohms) vs. current input in nanoamperes (nA) in an embodiment of a memory cell which has both a tunnel-junction control element and a tunnel-junction storage element. The plotted resistance **280** drops sharply upon anti-fuse breakdown **290** and drops further to zero upon breakdown **295** of the control-element tunnel junction. Thus, attention should be paid to over-voltage
30  control. Memory cell embodiments using a tunnel-junction storage element and employing a control element with both a silicon-rich insulator and a tunnel

junction are improved in breakdown resistance over those with only a tunnel-junction control element.

FIG. 11 is a cross-sectional side elevation overall view of a simplified embodiment of a multi-layer memory array **10**. In this embodiment, substrate
5  **300** may be a wafer of P-type silicon suitable for CMOS circuit fabrication, for example. A first level (M1) of patterned metallization **305** provides conductive lines for connection to vias **350**, for connection to control-select FET devices having control-select gates **360**, and for connecting through conductive lines **370** to sense amplifiers (not shown in FIG. 11). In FIG. 11, column conductors
10  **40** extend to left and right generally parallel to the plane of the drawing and row conductors **30** extend in the orthogonal direction generally perpendicular to the plane of the drawing. Three additional levels (e.g., second, third and fourth levels) of patterned metallization **310**, **320**, and **330** provide conductive lines for column conductors **40** and for connection to vias **350**. Two other levels of
15  patterned metallization between these provide the conductive lines for row conductors **30**. Interlayer dielectric (ILD) **340** isolates adjacent levels and adjacent cross-points within each level of the multi-layer memory array **10**. As indicated by dashed ellipse **380**, the area under the array is available for CMOS circuits in addition to the control-select devices mentioned above. While FIG. 11
20  shows only a few rows and columns for clarity of illustration, in actual practice a subarray may include a minimum of 1,000 rows and 1,000 columns, and a memory may include many subarrays.

FIG. 12 is a top plan view illustrating a simple embodiment of a chip layout or "floorplan" **400** for a memory array. A number of subarrays **410** may be
25  arranged as shown, with control circuitry **415** near their adjacent corners. Row-enable drive circuitry **420** may be arranged between subarrays **410** along one direction, and column decode circuitry **430**, including sense amplifiers, may be arranged along an orthogonal direction. Digital PLL circuitry **440**, digital control logic **450**, memory control **460**, and voltage regulation **470** (if required)
30  may be arranged as shown in FIG. 12 near interconnection pads **480** arranged along a chip edge. Many other layouts are possible.

FIG. 13 is a schematic block diagram of an embodiment of a row configuration for a memory array. Those skilled in the art will recognize that conventional details of row-enable drives **420** are omitted for clarity of illustration. Shown in FIG. 13 are row-enable lines **421** and **422**, row-enable bit circuitry **425**, bit-line-

5      select lines **490** and **491** (alternating), bit-enable lines **495** and **496**, and row levels 0 - 7 (respectively, **500 – 507**).

FIG. 14 is a simplified schematic diagram of an embodiment of a memory array, illustrating a write (programming) operation. In both FIGS. 14 and 15, the symbol enclosed in the dashed circles **510** and **610**, and replicated at each

10     cross-point, represents a memory cell comprising a series combination of a storage element and a control element, the latter including a tunnel junction and silicon-rich insulator. The cell enclosed in the dashed circle **510** is the cell which is being programmed. During a write operation, voltage V+ may be about two volts and voltage $V_a$ about 50 millivolts, for example. Arrow **520** represents row

15     current for the row of that cell. The four arrows **540** represent current in cells of adjacent cross-points (e.g., about one microampere). FET devices **505** are column-select devices. The unselected columns in this example are connected at **545** and **555** to their own sense amplifiers (not shown). Sense amplifier **550** for the cell being programmed is connected to the write-pulse control **560**.

20     When the row and column for cell **510** are selected, program current **530** may be about 20 microamperes, for example.

FIG. 15 is a simplified schematic diagram of an embodiment of a memory array corresponding to FIG. 14, but illustrating a read operation. In FIG. 15, the state of cell **610** is being read. Arrow **520** represents row current for the row of that

25     cell. Arrow **630** represents read current. The two arrows **640** represent current in cells of cross-points adjacent to cell **610** in the same row (e.g., about one nanoampere). FET devices **505** are again the column-select devices. Again, the unselected columns in this example are connected at **545** and **555** to their own sense amplifiers (not shown). Sense amplifier **550** is the sense amplifier

30     corresponding to the cell being read. During a read operation, voltage V+ may be about one volt and voltage $V_a$ about 50 millivolts, for example. Depending

on the state (ON or OFF) of cell **610** when the row and column for cell **610** are selected, read current **630** may be about ten microamperes for $I_{on}$ or about one microampere for $I_{off}$, for example.  Those skilled in the art will recognize that, while these examples (illustrated by FIGS. 14 and 15) are representative of an

5   array of about 1,000 rows and 1,000 columns using tunnel-junction storage elements, quantitative voltages and currents may differ for larger or smaller arrays and/or for arrays using other storage elements, such as chalcogenide state-change elements.  The present invention should not be construed as being limited to memory arrays using any particular type of storage element, nor

10   as being limited to memory arrays using voltages or currents similar to those in the examples described herein.

Another aspect of the invention is a memory cell including a storage element comprising a tunnel-junction anti-fuse, and including a control element coupled in series with the storage element, the control element comprising a patterned

15   silicon-rich insulator and a tunnel junction.  The patterned silicon-rich insulator of the control element injects current into the tunnel junction of the control element when the memory cell is selected and isolates the storage element when the memory cell is un-selected.  Such memory cells, like all the memory cell embodiments described herein, may be combined in a memory array having a

20   number of row conductors and a number of column conductors arranged to cross at cross-points, and the memory cell disposed at each cross-point.

Thus, another aspect of the invention is a memory array structure including a number of row conductors and a number of column conductors arranged to cross at cross-points and including a memory cell disposed at each cross-point,

25   each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, each storage element comprising a tunnel-junction anti-fuse, and each control element comprising a patterned silicon-rich insulator and a tunnel junction.

FABRICATION

FIG. 16 is a flow chart illustrating an embodiment of a method for fabricating a memory array.  Steps of this method embodiment are denoted by reference numerals **S10**, **S20**, ..., **S100**.  Some optional aspects of this method

5   embodiment are indicated in the usual manner by alternative paths through the flowchart.  If a substrate is used, a suitable substrate is provided in step **S10**.  The substrate **300** (shown in FIG. 11) may be a wafer of P-type silicon suitable for CMOS circuit fabrication, for example.  Those skilled in multi-layer memory integrated-circuit fabrication will recognize that the substrate for a particular

10  layer of memory may be provided by a previous level (i.e., by an interlayer dielectric over the previous memory layer, for example) so that a separate substrate need not necessarily be provided for memory layers after the first layer.  On the other hand, multi-layer memories may also be made by stacking multiple substrates, each carrying one or more memory-array layers.

15  In step **S20**, a first conductive layer is provided or deposited on the substrate.  The first conductive layer is patterned if necessary in step **S30** to form row conductors **30** or column conductors **40**.  A storage layer **50** is deposited in step **S40**.  A layer of silicon-rich insulator **60** is formed in step **S50,** and patterned in step **S55** if desired.  Silicon-rich insulator layer **60** may comprise

20  silicon-rich oxide (SRO), for example.  In step **S60**, a thin tunnel-junction layer **70** is formed, contiguous with the layer of silicon-rich insulator **60**.  In step **S70**, a second conductive layer is formed, contiguous with the tunnel-junction layer.  The second conductive layer is patterned in step **S80** to form column conductors **40** or row conductors **30**.

25  The step of depositing a thin silicon-rich oxide layer **60** may be performed by rapid thermal chemical vapor deposition (RTCVD) or by plasma-enhanced chemical vapor deposition (PECVD).  In a PECVD process, for example, the plasma may be formed in a mixture of $N_2O$ and silane ($SiH_4$) gases at 650°C and standard pressure.  The deposition may be performed at 600°C, but at a

30  higher pressure to achieve a reasonable deposition rate.  The ratio of $SiH_4$ gas to $N_2O$ gas is regulated to control the silicon content while depositing an oxide

$SiO_x$ where x is less than two.  The deposited silicon-rich oxide layer **60** has a composition which, alternatively, may be characterized by an elemental molar ratio of silicon to oxygen between about 0.51 and about one.  In other words, the process is controlled to provide an oxide having "excess" silicon, i.e., silicon

5    in excess of the amount required for stoichiometric silicon dioxide.  For example, the ratio of $SiH_4:N_2O$ may be about 1:20 for about 1% excess silicon in the SRO.  Typically, $SiH_4:N_2O$ ratios used are between about 1:10 for about 10% excess silicon and about 1:5 for about 50% excess silicon.  The step of depositing a thin tunnel-junction insulator layer **70** may also be performed by

10   rapid thermal chemical vapor deposition (RTCVD), by plasma-enhanced chemical vapor deposition (PECVD), or by atomic layer deposition (ALD) of $Al_2O_3$ or stoichiometric $SiO_2$.

For some embodiments, an interlayer dielectric (ILD) **120** is deposited (step **S90**).  Metal oxide **140** may serve as a functional equivalent for the layer of

15   interlayer dielectric (ILD) **120** in some embodiments, as shown in FIG. 8 and described in connection with that drawing.

Also, for some embodiments, a conductive middle electrode **130** is formed (step **S100**), contiguous with the layer of silicon-rich insulator **60**.  Formation of conductive electrode **130** may include patterning the electrode.  If necessary, an

20   additional step **S95** of planarizing the interlayer dielectric (ILD) is performed, e.g., by chemical-mechanical polishing (CMP).

Those skilled in the art will recognize from study and comparison of FIGS. 1 – 9 and 11 that the order of the steps in this fabrication method may be varied according to the type of embodiments to be fabricated.  FIG. 11 also shows that

25   metallization layers for row and column conductors **30** and **40** may be alternated in a multilayer memory structure.

Dimensions **L1 – L8** shown in cross-section drawings, FIGS. 2 – 7 represent typical dimensional relationships.  The actual dimensions achieved in practice depend on the lithographic technology employed, properties of the materials

30   used, and other known factors.  For example **L1**, **L2**, **L3**, and **L4** may all be

similar, less than about one micrometer, e.g., about 100 nanometers or less than 100 nanometers. **L8** may be about an order of magnitude smaller than **L1**, **L2**, **L3**, or **L4**. The thickness **L5** of storage layer **50** may be about 1 - 5 nanometers, for example. The effective thickness **L6** of silicon-rich insulator

5    layer **60** may be about 5 - 10 nanometers, for example. The thickness **L7** of tunnel-junction layer **70** may be about 3 - 5 nanometers, for example. Tunnel-junction layer **70** (with thickness **L7**) may be thicker in memory cell embodiments made in accordance with the present invention than in otherwise similar memory cells without silicon-rich insulator layer **60**. The additional

10    thickness improves layer yield. Thus, comparable characteristics can be achieved with higher layer yield, thereby reducing fabrication costs.

Thus, a practical aspect of the invention is a method for fabricating a memory cell **20** and corresponding methods for fabricating memory arrays **10** containing a number of such cells. Such method, as described above, includes steps of

15    providing a substrate **300**, depositing and patterning a first conductive layer **30** or **40** over the substrate, forming a storage layer **50**, forming a layer of silicon-rich insulator **60**, forming a tunnel-junction layer **70** over the layer of silicon-rich insulator, and forming and patterning a second conductive layer **30** or **40** over the tunnel-junction layer **70**. The method may also include steps of patterning

20    the layer of silicon-rich insulator, depositing an interlayer dielectric (ILD) **120**, planarizing the interlayer dielectric (ILD), forming a conductive middle electrode **130** contiguous with the layer of silicon-rich insulator and/or contiguous with storage layer **50**, and patterning the conductive middle electrode **130**. In one embodiment of such methods, the interlayer dielectric **120** is formed over

25    storage layer **50** and patterned, an opening is formed through the interlayer dielectric and extending to the storage layer **50**, and the opening through the interlayer dielectric is filled with conductive material to form a middle electrode **130** contiguous with the storage layer **50**. In some embodiments, middle electrode **130** is formed contiguous with the layer of silicon-rich insulator **60**.

30    The thin layer of insulator of the tunnel junction **70** may be a thin layer of aluminum oxide ($Al_2O_3$), silicon dioxide ($SiO_2$), silicon oxynitride, or other high-dielectric-constant (high-K) material, for example. Both the conductive row and

column conductors **30** and **40** and the middle electrode **130** may comprise any of a number of conductive materials, such as titanium or titanium nitride (TiN). Other conductive materials suitable for the conductive elements include aluminum, tungsten, gold, platinum, and other metals, and semiconductors such as silicon (e.g., crystalline, polycrystalline, microcrystalline, amorphous, or doped semiconductors).

For a memory array comprising many cells in one layer, all the cells may be made simultaneously with their interconnections provided in the row-conductor and column-conductor metallization layers. For a multi-layer memory array, a first layer may be made by this fabrication method and then the method may be repeated for subsequent layers with an interlayer dielectric between layers, each layer providing the substrate for the next layer. Conductive vias are used to interconnect memory layers. Thus, such a multilayer memory comprises a number of memory arrays arranged in memory layers with a number of interlayer dielectrics disposed to separate adjacent memory layers and with conductive vias selectively extending through the interlayer dielectrics to selectively interconnect memory cells of the memory arrays.

The memory cells of the multilayer memory may be organized in sets with the memory cells of each set at least partially aligned vertically with each other. The conductive vias interconnecting memory cells of each set may be interconnected electrically to form a common node for that set of memory cells. These conductive vias, interconnecting memory cells of each set, are at least partially aligned vertically, thus providing a vertical interconnection or pillar.

Another aspect of the invention is a method of controlling a memory cell of the type having an anti-fuse storage element. This method includes providing a patterned silicon-rich insulator combined with a tunnel junction to form a control element, whereby the memory cell is isolated when un-selected, coupling the control element in series with the anti-fuse storage element, and providing conductive elements for supplying current to selectively inject current from the silicon-rich insulator into the tunnel junction of the control element when selecting the memory cell. The memory cell structural embodiments and

memory array structural embodiments described above are specially adapted to use this method of control, and the fabrication methods described above are specially adapted to make such memory cells and memory arrays.

5  INDUSTRIAL APPLICABILITY

Devices made in accordance with the invention are useful in storage devices and have lower power requirements and larger subarray sizes than many memory devices available heretofore. They may be used in many applications that require storage of data, especially for storing large amounts of data. These
10  include applications in which the data may be written once, but must be read many times. The fabrication methods performed in accordance with the invention are specially adapted for making the devices described herein, with high yield and reduced cost through use of a minimal number of masks and through avoidance of very large driver devices.

15  Although the foregoing has been a description and illustration of specific embodiments of the invention, various modifications and changes thereto can be made by persons skilled in the art without departing from the scope and spirit of the invention as defined by the following claims. For example, as mentioned above, the order of method steps may be varied to some extent. Specifically,
20  for example, either the row conductors or column conductors may be deposited first on the substrate, and the order of steps is therefore varied in those two cases. Other functionally equivalent materials may be substituted for the specific materials described in the example embodiments. Specifically, current-injecting materials other than silicon-rich oxide (SRO) may be employed.